that its lock member is partially engaged, i.e., in the pushback-locked state; (3) two full lock switches 56 each indicating that its lock member is fully engaged, i.e., in the fully-locked state. In this state, the full lock switches indicating to the IDCU that the power need no longer be supplied to the motor 76.

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In the Drawings:

Please replace previously submitted formal Figures 1A, 1B, and 2 and previously submitted informal marked up Figures 1A, 1B and 2 with the even further corrected and marked-up informal versions of Figures 1A, 1B and 2 submitted herewith, wherein even further revisions to Figures 1A, 1B, and 2 have been indicated in red ink.

Please add informal drawings for Figures 3A-C, 4A-C, 5A-C, 6, 7A-B, 8, 9, 10A-C, 11, 12-C, 13, and 14A-E.

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In the Claims:

In accordance with 37 CFR 1.121(c), a "clean form" version of all claims amended herein is presented immediately hereafter. In further accordance with 37 CFR 1.121(c), a "marked up" version of each claim amended herein is set forth in Appendix B attached hereto.

Please amend Claims 4-9 to read as follows:

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4. (Amended) In an electrically noisy environment a self-locking memory circuit for a tri state data bus having multiple bit lines, said self-locking memory circuit comprising:

a non-clocked, non-inverting amplifier chip for connection to one of said bit lines; and

a resistor having a predetermined electrical resistance connected across said non-clocked, non-inverting amplifier chip;

wherein said self-locking memory circuit has upper and lower voltage thresholds that cause said self-locking memory circuit to change states when a level of voltage applied to said self-locking memory circuit passes through one of said thresholds.

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5. (Amended) In an electrically noisy environment a programmable system comprising:

a central processing unit;

a Digital Signal Processor for transceiving discrete electrical inputs; and

a tri state data bus electrically connecting said Digital Signal Processor to said central processing unit, said Digital Signal Processor and said central processing unit having different clock rates for accessing said tri state data bus; and

self-locking data bus circuits connected to respective bit lines of said tri state data bus for maintaining said respective bit lines of said tri state data bus in their last driven state during said access of said tri state data bus by said Digital Signal Processor and said central processing unit at said different rates.

6. (Amended) The programmable system according to Claim 5, wherein said programmable system further comprises:

a Complex Programmable Logic Device for transceiving discrete electrical signals;

[a] wherein said tri state data bus electrically interconnects said central processing unit, said Digital Signal Processor, and said Complex Programmable Logic Device, said Digital Signal Processor and said Complex Programmable Logic Device having clock rates for accessing said tri state data bus that are different from a clock rate at which said central processing unit accesses said tri state data bus; and

B10 wherein said programmable system additionally includes self-locking data bus circuits connected to respective bit lines of said tri state data bus for maintaining said respective bit lines of said tri state data bus in their last driven state during access of said tri state data bus by said Digital Signal Processor, said Complex Programmable Logic Device, and said central processing unit at said different rates.

7. (Amended) The programmable system according to Claim 5, wherein each of said self-locking data bus circuits includes:

a non-clocked, non-inverting amplifier chip for connection to one of said bit lines; and

a resistor having a predetermined electrical resistance connected across said non-clocked, non-inverting amplifier chip;

wherein each of said self-locking data bus circuits has upper and lower voltage thresholds that cause respective ones of said self-locking data bus circuits to change states when a level of voltage applied to said respective ones of said self-locking data bus circuits passes through one of said thresholds.

8. (Amended) In an electrically noisy environment a programmable system comprising:

a central processing unit;

a Complex Programmable Logic Device for transceiving discrete electrical inputs; and

B10 a tri state data bus electrically connecting said Complex Programmable Logic Device to said central processing unit, said Complex Programmable Logic Device and said central processing unit having different clock rates for accessing said tri state data bus; and

self-locking data bus circuits connected to respective bit lines of said tri state data bus for maintaining said respective bit lines of said tri state data bus in their last driven state during access of said tri state data bus by said Complex Programmable Logic Device and said central processing unit at said different rates.

9. (Amended) The programmable system according to Claim 8, wherein each of said self-locking data bus circuits includes: